IN THE CLAIMS:

1-32. (Canceled).

33. (Original) A driver circuit for a display, comprising:

k voltage levels, where k is at least $2^{(n-1)}$;

an input receiving a digital input data having n bits for selecting one of the k voltage levels for driving the circuit;

an output having a first side;

a plurality of digital signal lines coupled to the digital input data; and

a plurality of transistor groups, each transistor group formed by a plurality of serially coupled transistors, each transistor group being coupled to a separate one of the voltage levels and the output from the first side of the output, each transistor group having n controllable transistors, each controllable transistor having a gate controlled by one of the digital signal lines;

wherein the number of the plurality of digital signal lines on the first side of the output is less than 2n, with the digital signal lines comprising a first set of digital signal lines associated with a first set of digital bits and a second set of digital signal lines associated with a second set of digital bits, the second set of digital bits being inverted from the first set of digital bits; and

wherein n is a positive integer greater than 1.

34. (Original) The circuit of claim 33, wherein the plurality of digital signal lines are polysilicon lines.

35. (Original) The circuit of claim 33, wherein the number of the plurality of digital signal lines on the first side of the output is equal to 2n-1.

36. (Original) The circuit of claim 33, wherein the number of the plurality of digital signal lines on the first side of the output is equal to 2n-2.

37. (Original) The circuit of claim 33, wherein the number of the digital signal lines on the first side of the output is an odd number.

38. (Original) The circuit of claim 33, wherein each transistor group has a total of m transistors, with m being a positive integer that is greater than n.

39. (Original) A driver circuit for a display, comprising:

k voltage levels, where k is at least $2^{(n-1)}$;

an input receiving a digital input data having n bits for selecting one of the k voltage levels for driving the circuit;

an output having a first side;

a plurality of digital signal lines coupled to the digital input data; and

a plurality of transistor groups, each transistor group formed by a plurality of serially coupled transistors, each transistor group being coupled to a separate one of the voltage levels and the output from the first side of the output, each transistor group having n controllable transistors, each controllable transistor having a gate controlled by one of the digital signal lines;

a plurality of blocking transistors positioned between the input and selected digital signal lines, with at least one of the digital signal lines being coupled to a gate of each of the blocking transistors for controlling each of the blocking transistors; and

wherein n is a positive integer greater than 1.

40. (Original) The circuit of claim 39, further including a buffer positioned between the input and each digital signal line, wherein the buffers for the digital signal lines that control the blocking transistors are larger in size than the other buffers.

41. (Original) The circuit of claim 39, wherein each blocking transistor is either a NMOS switching gate or a CMOS transfer gate.

42. (Original) The circuit of claim 39, wherein the number of the plurality of digital signal lines on the first side of the output is an odd number.

43. (Original) The circuit of claim 39, wherein the number of the plurality of digital signal lines on the first side of the output is equal to 2n-1.

44. (Original) The circuit of claim 39, wherein the number of the plurality of digital signal lines on the first side of the output is equal to 2n-2.

45. (Original) The circuit of claim 39, wherein each transistor group has a total of m transistors, with m being a positive integer that is greater than n.

46. (Original) A driver circuit for a display, comprising:

k voltage levels, where k is at least $2^{(n-1)}$;

an input receiving a digital input data having n bits for selecting one of the k voltage levels for driving the circuit;

an output having a first side;

a plurality of digital signal lines coupled to the digital input data; and

a plurality of transistor groups, each transistor group formed by a plurality of serially coupled transistors, each transistor group being coupled to a separate one of the voltage levels and the output from the first side of the output, each transistor group having n controllable transistors, each controllable transistor having a gate controlled by one of the digital signal lines;

wherein the number of the plurality of digital signal lines on the first side of the output is equal to 2n-2; and

wherein n is a positive integer that is greater than 1.

47. (Original) The circuit of claim 46, wherein the plurality of digital signal lines are polysilicon lines.

48. (Original) The circuit of claim 46, wherein a first of the digital signal lines is discontinued between two adjacent active regions to form a first digital segment carrying the digital signal, and a second digital segment carrying a digital signal that is inverted from the digital signal of the first digital segment.

49. (Original) The circuit of claim 46, further including a plurality of blocking transistors positioned between the input and selected digital signal lines, with at least one of the digital signal lines being coupled to a gate of each of the blocking transistors for controlling each of the blocking transistors.

50.-(Original) The circuit of claim 49, further including a buffer positioned between the input and each digital signal line, wherein the buffers for the digital signal lines that control the blocking transistors are larger in size than the other buffers.

51. (Original) A driver circuit for a display, comprising:

k voltage levels, where k is at least $2^{(n-1)}$;

an input receiving a digital input data having n bits for selecting one of the k voltage levels for driving the circuit;

an output having a first side;

a plurality of digital signal lines coupled to the digital input data; and

a plurality of transistor groups, each transistor group formed by a plurality of serially coupled transistors, each transistor group being coupled to a separate one of the voltage levels and the output from the first side of the output, each transistor group having n controllable transistors, each controllable transistor having a gate controlled by one of the digital signal lines;

at least one level-shifter, each level-shifter associated with a digital signal line; and

wherein n is a positive integer greater than 1.

52. (Original) The circuit of claim 51, wherein the plurality of digital signal lines are polysilicon lines.

53. (Original) The circuit of claim 51, further including a plurality of blocking transistors positioned between the input and selected digital signal lines, with at least one of the digital signal lines being coupled to a gate of each of the blocking transistors for controlling each of the blocking transistors.

54. (Original) The circuit of claim 51, wherein a first of the digital signal lines is discontinued between two adjacent active regions to form a first digital segment carrying the digital signal, and a second digital segment carrying a digital signal that is inverted from the digital signal of the first digital segment.

55. (Original) The circuit of claim 51, wherein the digital signal line has at least two discontinued segments, with a level shifter coupling between the discontinued segments.